EXHIBIT 1 TO
RESPONSE OF DEC. 1 2002
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PowerPC™ 601

RISC Microprocessor User's Manual

IBM®

07	06	05	04	11 03	12 02	13 01	14 00
21 0F	22 0E	23 0D	24 0C	25 0B	26 0A	27 09	28 08
'D' 17	'C' 16	'B' 15	'A' 14	31 13	32 12	33 11	34 10
1F	1E	51 1D	52 1C	1B	'G' 1A	'F' 19	'E' 18
				61 23	62 22	63 21	64 20

Figure 2-33. Little-Endian Mapping of Structure *S*

2.4.5 PowerPC Byte Ordering

The default mapping for PowerPC processors is big-endian. Little-endian mode can be selected after a hard reset by setting the LM bit in the HID0 register in the PPC601 through the use of the **mtspr** instruction in the hard reset handler. The location of the bit is unique for each PowerPC processor.

2.4.6 PowerPC Data Memory with LM Set

One might expect that with the LM bit set (little-endian mode), that the system would have to perform two-, four-, or eight-way byte swaps when transferring a half word, word, or double word between memory and a register. However, the PowerPC architecture emulates little-endian byte ordering by manipulating the three low-order bits of the effective address. No bytes are swapped and individual multiple-byte scalars appear in memory in big-endian order. Setting LM adjusts the way effective addresses are computed without affecting the transfer of data between memory and registers, which is unencumbered by the need for multiplexers to swap bytes.

2.4.6.1 Aligned Scalars

For the load and store instructions listed in Table 2-28, the effective address is computed as specified in the instruction descriptions in Chapter 3, "Addressing Modes and Instruction Set Summary," and is modified as shown in Table 2-29.

Table 2-28. Load/Store Instructions for Data Aligned on Natural Boundaries

Mnemonic	Instruction
lbz	Load Byte and Zero
lbzu	Load Byte and Zero with Update
lbzux	Load Byte and Zero with Update Indexed
lbzx	Load Byte and Zero Indexed
lfd	Load Floating-Point Double-Precision
lfdu	Load Floating-Point Double-Precision with Update